LISTING OF THE CLAIMS

Please amend the Claims as shown below. This listing of claims will replace all prior versions and listings of claims in the Application.

1. (Currently Amended) A semiconductor structure comprising:

a pad area wherein said pad area comprises:

a substrate;

a first layer of metal disposed above said substrate wherein said active device is disposed below said first layer of metal;

a second layer of metal disposed above said first layer of metal;

a layer of dielectric disposed between said first metal layer and said second metal layer wherein said dielectric comprises tetraoxysilane;

a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer; and

one or more subsequent layers of metal between said first and said second metal layers, wherein said via comprises one or more of a plurality of vias and wherein one or more of said vias electrically couples one or more of said subsequent layers with one or more of each other, said first and said second layers of metal; and

an active device of said semiconductor structure disposed below said pad area and within said substrate wherein one or more of said vias electrically couples said active device with one or more of said metal layers.

2. (Currently Amended) The semiconductor structure as recited in Claim 1 wherein said active device ~~component~~ comprises a transistor.

3. (Original) The semiconductor structure as recited in Claim 1 wherein a component of said semiconductor structure performs a logic function.

4. (Original) The semiconductor structure as recited in Claim 1 wherein a component of said semiconductor structure performs a memory function.

5. (Original) The semiconductor structure as recited in Claim 1 wherein said active device comprises a first device, said semiconductor structure further comprising:

a non-pad area bounded at least in part by said pad area; and

a second device disposed within said non-pad area.

6. (Original) The semiconductor structure as recited in Claim 5 wherein said first and said second devices perform a similar function.

7-9. (Cancelled)

10. (Currently Amended) A pad area apparatus for a semiconductor structure comprising:

a substrate;

a first layer of metal disposed above said substrate;

a second layer of metal disposed above said first layer of metal;

a layer of dielectric disposed between said first metal layer and said second metal layer wherein said dielectric comprises tetraoxysilane;

a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layers; and

one or more layers of metal disposed between said first and said second metal layers, wherein said via comprises one or more of a plurality of vias and wherein one or more of said vias electrically couples one or more of said subsequent layers with one or more of each other, said first and said second layers of metal; and

an active component wherein said active component is disposed within said substrate and wherein one or more of said vias electrically couples said active device with one or more of said metal layers.

11-21. (Cancelled)